



ASMEX.1

PATENT

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Raaijmakers et al.

Appl. No. : 09/764711

Filed : January 18, 2001

For : METHOD OF DEPOSITING  
SILICON WITH HIGH STEP  
COVERAGE

Examiner : Angel Roman

) Group Art Unit 2812

) I hereby certify that this correspondence and all  
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) Arlington, VA 22202, on

) July 8, 2002

) (Date)

) Adeel S. Akhtar  
) Adeel S. Akhtar, Reg. No. 41,394RESPONSE TO FINAL OFFICE ACTION

United States Patent and Trademark Office  
P.O. Box 2327  
Arlington, VA 22202

Dear Sir:

In response to the Final Office Action mailed on May 9, 2002, Applicants respectfully request reconsideration in view of the amendments and remarks below.

REMARKS

In the Final Office Action mailed on May 9, 2002, the Examiner rejected all pending claims. Applicants respectfully request reconsideration of the rejections in view of the remarks contained herein.

Anticipation Rejections

The Examiner has rejected Claims 33 and 35-37 as being anticipated by Vo (U.S. Patent No. 5,097,381A).

Regarding Vo, the Examiner stated that "Vo discloses an integrated capacitor formed in a trench having a width no more than about 0.25 micrometers ... and an aspect ratio greater than about 20:1 (see column 5, lines 35-45), comprising; a dielectric layer 54 lining the trench; and a conductively doped polysilicon layer 52 (see column 5, lines 20-30) filling the trench."

#8 / Response 7-23-02

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